Remarks

The present amendment responds to the Official Action dated February 28, 2006. A petition for a two month extension of the time to respond and authorization to charge Deposit Account No. 50-1058 the $450 fee for this extension accompany this amendment. The Official Action rejected claim 49 under 35 U.S.C. 101 on the grounds of double patenting with respect to claim 20 of U.S. Patent No. 6,760,831. Claims 6-9, 48-52 and 56-73 were rejected on the ground of non-statutory obviousness-type double patenting based on the same claim 20. Claims 6-8 and 56-58 were rejected under 35 U.S.C. 102(b) based on Muhlke et al., "Effective Complier Support for Predicated Execution Using the Hyperblock" (Muhlke). Claims 60-68 and 69-73 were rejected under 35 U.S.C. 112, second paragraph, as indefinite. Claims 9 and 59 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These grounds of rejection are addressed below. Claims 8, 50, 52, 58, and 65-67 have been canceled, claims 6, 56, and 69 have been amended to be more clear and distinct, and new claims 74-80 have been added. Claims 6, 7, 9, 49, 51, 56, 57, 59-64, and 68-80 are presently pending.

35 U.S. C. 101 Same Invention Double Patenting Rejection of Claim 49

While the similarity of claim 49 and claim 20 of commonly owned U.S. Patent No. 6,760,831 might support an obviousness type double patenting rejection like that made for claims 6-9, 48-52 and 56-73, reconsideration and withdrawal of the "same invention" rejection are requested on the grounds urged below. As stated by MPEP § 804 at p. 800-20, "same invention"

means identical subject matter. The subject matter of the two claims is not identical as seen by a side by side comparison of the next to the last elements of both these claims as follows:

Present Claim 49	Claim 20 of U.S. Patent No. 6,760,831
each execution unit having an arithmetic flag (ACF) generation unit for providing a **Boolean combination of a present selected state with a previous state** (emphasis added)	each execution unit having an arithmetic flag (ACF) generation unit for providing a **present selected state of plurality of arithmetic condition flags (ACFs)** (emphasis added)

Obviousness-Type Double Patenting Rejection of Claims 6-9, 48-52

A terminal disclaimer is submitted to overcome this rejection, and provisionally the rejection of claim 49 if that rejection is withdrawn in favor of an obviousness-type double patenting rejection.

Section 112 Rejections of Claims 60-68 and 69-73

With respect to both claims 60 and 69, the Official Action states "it is unclear what the antecedent basis for the "processing element", clarification or withdrawal of this objection as line 5 of claim 60 clearly recites "a processing element" and lines 2 and 3 of claim 69 also recites "a processing element". Claims 60 and 69 have been amended to be more clear and distinct and address the remaining Section 112 objections.

The Art Rejections

As addressed in greater detail below, Muhlke does not support the Official Action's reading of it and the rejections based thereupon should be reconsidered and withdrawn. Further,

the Applicant does not acquiesce in the analysis of Muhlke made by the Official Action and respectfully traverses the Official Action's analysis underlying its rejections.

Muhlke describes a predicated execution architecture using a predicate register file storing predicates that are specified by specific instructions that identify setting a predicate. Muhlke states that "The contents of a predicate register may only be modified by one of 3 operations: stuff, stuff_bar, or brtop." (emphasis added) Muhlke, page 46, first sentence of the first paragraph in the right column under Figure 1. Muhlke then proceeds to describe additional instructions which may be used to modify the predicate registers, for example a pred_clear instruction, various types of compare instructions, and pred_ld instruction. Muhlke, page 47, second paragraph from the top in the left column. In all instructions presented by Muhlke, there is a direct relationship between one of these instructions and a specified predicate register. Each instruction directly affects the setting of a predicate register as a result of its execution.

In contrast, the present invention uses an indirect VLIW architecture in which a load VLIW instruction is used to load instructions in a separate VLIW memory and an execute VLIW instruction is used to indirectly select a VLIW from the VLIW memory for execution. A VLIW, in the context of the present invention, contains a set of instructions with each instruction associated with an execution unit. Both the load VLIW and the execute VLIW instructions contain encodings which are used to identify an execution unit of the plurality of execution units associated with a selected VLIW that can affect an arithmetic condition flag (ACF). As an example, an execute VLIW instruction is a first instruction which identifies in a unit affecting field (UAF) the unit, such as the data select unit (DSU), which is allowed to affect the ACFs. A

DSU instruction is a second instruction which is one of the instructions in a VLIW. The second instruction specifies a condition, such as a result equal zero (Z value) condition, which occurs as a result of executing the DSU instruction on the DSU execution unit. The condition, (Z value), is used to set one of the flags of the ACF since it was allowed to do so by the UAF field of the first instruction. This mechanism allows a program to identify in a first instruction one of a plurality of VLIW execution units that is permitted to affect an ACF and further allows the identification, in a second instruction, of a condition, resulting from the identified execution unit executing, for setting the ACF. Present invention, pages 22-23 VLIW Conditional Execution section and pages 27-29 paragraphs beginning under Table 11. Muhlke does not teach and does not make obvious the presently claimed combination of executing first and second insertions to support conditional execution in a VLIW based array processor of claim 6 which reads as follows:

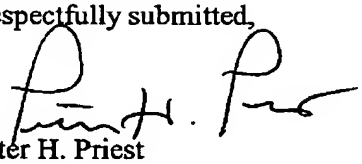
> A method of **supporting conditional execution in a very long instruction word (VLIW) based array processor,** the method comprising:
> **executing a first instruction that identifies an execution unit** of a plurality of execution units, the identified execution unit to affect the value of an arithmetic condition flag (ACF), wherein the identified execution unit is associated with a second instruction being one of the instructions in a VLIW;
> **executing the second instruction on the identified execution unit, the second** instruction identifies a condition resulting from the execution of the second instruction; and
> setting the identified condition in the ACF. (emphasis added)

Claim 56 is amended in a similar manner to claim 6 placing it in order for allowance.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,



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